What is Claimed is:

1. A test mode control device using a nonvolatile ferroelectric memory, comprising:

a first reference voltage controller for outputting a reference voltage control signal having a predetermined level of voltage in response to a reference input signal;

a reference register unit for programming a code to control a reference voltage in a nonvolatile ferroelectric memory, and for outputting a register control signal including information on a test mode or normal operation mode depending on the programmed code;

a path control means for selectively outputting an external control signal inputted externally in the test mode in response to the register control signal, and for selectively outputting the reference voltage control signal in the normal operation mode; and

a second reference voltage controller for controlling a voltage level of a reference voltage under the same condition with a cell array block in response to an output signal of the path control means.

2. The device according to claim 1, wherein the first reference voltage controller comprises:

a first driver for initializing a first node corresponding to a sub-bitline of the cell array block in activation of the reference input signal; and

a nonvolatile ferroelectric capacitor connected between a plate reference voltage control signal input terminal and the first node.

3. The device according to claim 1, wherein the path control means comprises:

a first path controller for outputting an output signal from the first reference voltage controller in response to a first register control signal activated in the normal operation mode; and

a second path controller for outputting the external control signal in response to a second register control signal activated in the test mode.

4. The device according to claim 1, wherein the reference register unit comprises:

a program command processor for outputting a command signal to code a program command in response to a write enable signal, a chip enable signal, an output enable signal and a reset signal;

a program register controller for performing a logic

operation on input data, a power-up detecting signal and the command signal and outputting a write control signal and a cell plate signal;

a program register array comprising a nonvolatile ferroelectric memory device, for outputting the programmed code in response to a pull-up enable signal, a pull-down enable signal, the write control signal and the cell plate signal; and

a reset circuit unit for outputting the reset signal into the program register controller in a power-up mode.

5. The device according to claim 4, wherein the program command processor comprises:

a logic unit for performing a logic operation on the write enable signal, the chip enable signal, the output enable signal and the reset signal;

a flip-flop unit for sequentially flip-flopping toggle of the output enable signal corresponding to an output signal from the logic unit and outputting the command signal; and

an overtoggle detecting unit for detecting overtoggle of the output enable signal.

6. The device according to claim 5, wherein the

logic unit comprises:

a first NOR gate for performing a NOR operation on the write enable signal and the chip enable signal;

a first AND gate for performing an AND operation on an output signal from the first NOR gate and the output enable signal; and

a second AND gate for performing an AND operation on the output signal from the first NOR gate, an inverted reset signal and an output signal from the overtoggle detecting unit.

7. The device according to claim 5, wherein the flip-flop unit comprises a plurality of flip-flops having data input nodes and output nodes connected in series to output the command signal from an output terminal of the last flip-flop, and to flip-flop the output enable signal in response to an activation synchronizing signal applied from the logic unit.

8. The device according to claim 4, wherein the program register controller comprises:

a third AND gate for performing an AND operation on the command signal and the output data;

a first delay unit for non-inverting and delaying an

output signal form the third AND gate;

a second NOR gate for performing a NOR operation on the output signal from the third AND gate and an output signal from the first delay unit;

a second delay unit for delaying an output signal from the second NOR gate and outputting the write control signal;

a third NOR gate for performing a NOR operation on the output signal from the second NOR gate and the power-up detecting signal; and

a third delay unit for inverting and delaying an output signal from the third NOR gate and outputting the cell plate signal.

9. The device according to claim 4, wherein the program register array comprises:

a pull-up driver for pulling up a power voltage when the pull-up enable signal is enabled;

a first driving unit, cross-coupled to both ends of a program register, for driving a voltage applied from the pull-up driver;

a write enable controller for outputting the reset signal and a set signal into both ends of the program register in response to the write control signal;

a ferroelectric capacitor unit for generating voltage difference in both ends of the program register in response to the cell plate signal;

a pull-down driver for pulling down a ground voltage when the pull-down enable signal is enabled; and

a second driving unit, cross-coupled to both ends of the program register, for driving a voltage applied from the pull-down driver.

10. The device according to claim 1, wherein the second reference voltage controller comprises:

a third driving unit for outputting a ground voltage into a second node corresponding to a main bitline of the cell array block when an output signal applied from the path control means is activated;

a second driver for outputting a power voltage into the second node corresponding to a main bitline load controller of the cell array block;

a fourth driving unit for selectively outputting a voltage of the second node corresponding to a column selecting controller of the cell array block;

a capacitor corresponding to a delay element of the second node; and

a third driver for outputting a power voltage into

the second node in response to a main bitline pull-up control signal corresponding to a main bitline pull-up controller of the cell array block.

11. A test mode control device using a nonvolatile ferroelectric memory, comprising:

a first timing controller for controlling timing of an address transition detecting signal;

a timing control register unit for programming a code to control timing of a cell array block driving control signal in a nonvolatile ferroelectric memory, and outputting a register control signal including information on a test mode or normal operation mode depending on the programmed code;

a path control means for selectively outputting an external control signal inputted externally in the test mode in response to the register control signal, and selectively outputting an output signal from the first timing controller in the normal operation mode; and

a second timing controller for controlling timing of the cell array block driving control signal in response to an output signal from the path control means.

12. The device according to claim 11, wherein the

first timing controller comprises:

an inverter chain for delaying the address transition detecting signal for a predetermined time; and

a capacitor connected to each node of the inverter chain.

13. The device according to claim 11, wherein the path control means comprises:

a third path controller for outputting an output signal from the first timing controller in response to a first register control signal activated in the normal operation mode; and

a fourth path controller for outputting the external control signal in response to a second register control signal activated in the test mode.

14. The device according to claim 11, wherein the timing control register unit comprises:

a program command processor for outputting a command signal to code a program command in response to a write enable signal, a chip enable signal, an output enable signal and a reset signal;

a program register controller for performing a logic operation on input data, a power-up detecting signal and

the command signal, and outputting a write control signal and a cell plate signal;

a program register array comprising a nonvolatile ferroelectric memory device, for outputting the programmed code in response to a pull-up enable signal, a pull-down enable signal, the write control signal and the cell plate signal; and

a reset circuit unit for outputting the reset signal into the program register controller in a power-up mode.

15. The device according to claim 11, wherein the second timing controller comprises an OR gate for performing an OR operation on the address transition detecting signal and an output signal from the path control means and for outputting the cell array block driving control signal.

16. A test mode control device using a nonvolatile ferroelectric memory, comprising:

a plurality of pads to receive a control signal and an address;

a plurality of buffers for buffering the control signal and the address inputted from the plurality of pads;

a pad register unit for programming a code for

assignment of the control signal and the address inputted into the pad in a nonvolatile ferroelectric memory, and changing a connection path between the plurality of pads and the plurality of buffers depending on the programmed code; and

a path control means for controlling connection between the plurality of pads and the plurality of buffers in response to the register control signal.

17. The device according to claim 16, wherein the path control means comprises:

a first path controller for connecting a control pad to a control buffer and an address pad to an address buffer in activation of a first register control signal; and

a second path controller for connecting the control pad to the address buffer and the address pad to the control buffer in activation of a second register control signal having an opposite phase to the first register control signal.

18. The device according to claim 17, wherein the first path controller comprises:

a first switching device, connected between the control pad and the control buffer, to be switched by the

first register control signal; and

a second switching device, connected between the address pad and the address buffer, to be switched by the first register control signal.

19. The device according to claim 17, wherein the second path controller comprises:

a third switching device, connected between the address pad and the control buffer, to be switched by the second register control signal; and

a fourth switching device, connected between the control pad and the address buffer, to be switched by the second register control signal.

20. The device according to claim 16, wherein the pad register unit comprises:

a program command processor for outputting a command signal to code a program command in response to a write enable signal, a chip enable signal, an output enable signal and a reset signal;

a program register controller for performing a logic operation on input data, a power-up detecting signal and the command signal, and outputting a write control signal and a cell plate signal;

a program register array comprising a nonvolatile ferroelectric memory device, for outputting the programmed code in response to a pull-up enable signal, a pull-down enable signal, the write control signal and the cell plate signal; and

a reset circuit unit for outputting the reset signal into the program register controller in a power-up mode.